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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,561	09/12/2003	Jeong-Wook Lee	030681-572	5312

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BUCHANAN, INGERSOLL & ROONEY PC
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

EXAMINER	
MULPURI, SAVITRI	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,561	LEE ET AL.	
	Examiner	Art Unit	
	Savitri Mulpuri	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE(21 July 2006)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/21/2006 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-15, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsakalakos et al (US 20040077156) in combination with Zhang et al (2003/0010971 A).

Tsakalakos et al teaches growing GaN based compound semiconductor layer in the nanoholes. Tsakalakos et al also teaches forming nanoholes in the mask of dielectric material "302" (see fig. 4) or mask formed from first semiconductor layer of GaN based material "102" called as defective buffer layer (see fig. 5). Growing a second GaN layer in the mask formed from first semiconductor of GaN layer"102",

wherein the second GaN layer is grown until the GaN defective buffer mask is fully covered.

Tsakalakos et al teaches forming nanoholes in the mask "302" by using block copolymer. Tsakalakos et al do not teach a method of manufacturing a device by the following process steps: Sequentially stacking a first semiconductor layer, a mask layer and a metal layer on a substrate: anodizing the metal layer to transform metal layer into a metal oxide layer including a plurality of nanoholes; etching the mask layer using the metal oxide layer as an etch mask until the nanoholes are extended to the surface of the first semiconductor layer; removing the metal oxide layer by etching; before regrowing a second semiconductor layer within the manholes and on the mask.

Zhang et al teaches a method of manufacturing a device by the following process steps:

Sequentially stacking a first semiconductor layer "82'", a mask layer"96" and a metal layer "84"on a substrate (see fig. 5B);

anodizing the metal layer to transform metal layer into a metal oxide layer "86" including a plurality of nanoholes"88"(see fig.5C)

etching the mask layer using the metal oxide layer as an etch mask until the nanoholes "98" are extended to the surface of the first semiconductor layer (see fig.5D);

removing the metal oxide layer by etching; and depositing a second semiconductor layer "90a,90b,92 within the nanoholes and on the mask "96" (see fig. 5D- 5F and para. 0041). Zhang et al indirectly teach filling the quantum dots "90 a, 90 b" to either completely or partially fill the nanoholes by disclosing, in some

embodiments, quantum dots 90 a, 90 b are grown to completely fill nanoholes (see para0041). When quantum dots are partially filled in the nanoholes semiconductor layer "92" is grown in the nanoholes and on the top of the mask "96, which supports amended limitation in step "f"

In re. to cl. 2, the diameter of the naonoholes is 10 to 100 nm (para. 0038, lines 1-8).

In re. to cl. 3, Zhang et al the area of the holes are inherently less than 50 percent of the whole area by showing metal oxide "86" wider than nanoholes "88" (see the fig. 5 C)

In re cl. 4 mask thicknesses must inherently same as claimed thickness., because both Zhang et al and instant invention has same goal of forming nanoholes with same diameter.

In re. to cl.5, Zhang et al uses a substrate made of GaAs and semiconductor layer made of AlGaAs and both GaAs and AlGaAs have different lattice constants.

In re. to cl. 6 the substrate is GaAs(see fig.5A)

In re. to cl.9 , cl. 11 the mask is dielectric layer of silicon oxide '"96"

In re. to cl. 12-14 Zhang further use refractory metal such titanium along with aluminum as metal layer, wherein titanium along with aluminum for good adhesion(see page 4, para. 0029).

In re. to cl. 15 etching is ion etching, which is dry etching (see para 0028, last 6 lines).

With respect to claims 7 and 8, Zhang et al do not teach growing GaN based compound semiconductor layer in the nanoholes. With respect to claim 9, 10, Zhang et al do not teach polycrystalline semiconductor layer is polysilicon or polycrystalline silicon.

It would have been obvious to one of ordinary skill in the art, in the invention of Tsakalakos et al to sequentially form a mask layer and a metal layer on sequentially formed GaN based semiconductor layers grown on a substrate: anodizing the metal layer to transform metal layer into a metal oxide layer including a plurality of nanoholes; etching the mask layer using the metal oxide layer as an etch mask until the nanoholes are extended to the surface of the first semiconductor layer; removing the metal oxide layer by etching before regrowing a second semiconductor layer within the manholes and on the mask, as alternative to form nanoholes in the mask using block copolymer in the invention of Tsakalakos et al because the purpose of both inventions Tsakalakos et al and Zhang et al teaches forming nanoholes in the mask and then growing compound semiconductor based layer on the mask with naonoholes to reduce defects or dislocations.

Response to Arguments

Applicant's arguments with respect to claims 1-15,18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Savitri Mulpuri whose telephone number is 571-272-1677. The examiner can normally be reached on Mon-Fri from 8 a.m to 4.30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt, can be reached on 571-272-1783. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Savitri Mulpuri
Primary Examiner
Art Unit 2812